LISTING OF CLAIMS

Following is a listing of claims which listing supersedes any previously submitted listing.

Claims 1 – 19 (Cancelled)

Claim 20. (Original) A MOS transistor comprising:

a T-shaped gate electrode disposed on a semiconductor substrate;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the gate electrode;

a low-concentration impurity region formed in the semiconductor substrate at both sides of the gate electrode;

a high-concentration impurity region formed in the semiconductor substrate next to the lower spacer; and

a mid-concentration impurity region disposed between the high- and low- concentration impurity regions.

Claim 21. (Original) The MOS transistor as claimed in claim 20, wherein the gate electrode comprises:

lower and upper conductive layer patterns that are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern so as to have an undercut region at a lower portion of the upper conductive layer pattern.

Claim 22. (Original) The MOS transistor as claimed in claim 21, wherein the L-shaped lower spacer further comprises a horizontal extension filling the undercut region.

Claim 23. (Original) The MOS transistor as claimed in claim 21, wherein the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other.

Claim 24. (Original) The MOS transistor as claimed in claim 21, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

Claim 25. (Original) The MOS transistor as claimed in claim 21, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

Claim 26. (Original) The MOS transistor as claimed in claim 20, further comprising a surface insulating layer intervened between the gate electrode and the lower spacer.